

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

## Scheme of Teaching and Examination

### B.E. VI Semester

### Electronics & Telecommunication Engineering

Sl. No.	Board of Study	Code No.	Subjects	Period Per Week			Scheme of Exam			Total Marks	Credit L+(T+P)/2
				L	T	P	Theory/ Practical				
							ESE	CT	TA		
1	Electronics & Telecommunication	328651(28)	Digital Signal Processing	3	1	-	80	20	20	120	4
2	Electronics & Telecommunication	328652(28)	Electronic Circuit Design	3	1	-	80	20	20	120	4
3	Electronics & Telecommunication	328653(28)	Microcontroller & Embedded	3	1	-	80	20	20	120	4
4	Electronics & Telecommunication	328654(28)	VLSI Design	3	1	-	80	20	20	120	4
5	Electronics & Telecommunication	328655(28)	Information Theory & Coding	3	1	-	80	20	20	120	4
6	<i>Refer Table -1</i>		Professional Elective -I	3	-	-	80	20	20	120	3
7	Electronics & Telecommunication	328661(28)	Digital Signal Processing Lab	-	-	2	40	-	20	60	1
8	Electronics & Telecommunication	328662(28)	Electronic Circuit Design Lab	-	-	4	40	-	20	60	2
9	Electronics & Telecommunication	328663(28)	Microcontroller & Embedded	-	-	4	40	-	20	60	2
10	Electronics & Telecommunication	328664(28)	VLSI Design Lab	-	-	4	40	-	20	60	2
11	Management	300665(76)	Managerial Skills	-	-	2	-	-	40	40	1
12			Library	-	-	1	-	-	-	-	-
<b>TOTAL</b>				<b>18</b>	<b>5</b>	<b>17</b>	<b>640</b>	<b>120</b>	<b>240</b>	<b>1000</b>	<b>31</b>

**L:** Lecture                      **T:** Tutorial                      **P:** Practical  
**ESE:** End Semester Examination      **CT:** Class Test              **TA:** Teachers' Assessment

**Note:** Industrial Training of eight weeks is mandatory for B.E. students. It is to be completed in two equal parts. The first part must have been completed in summer after IV semester. The second part to be completed during summer after VI semester after which students have to submit a training report which will be evaluated by college teachers during B.E. VII semester.

**Table 1**  
**Professional Elective – I**

Sl. No.	Board of Study	Code	Subject
1	Electronics & Telecom.	328671(28)	Internet & Web Technology
2	Electronics & Telecom.	328672(28)	Operating System
3	Electronics & Telecom.	328673(28)	Biomedical Electronics
4	Electronics & Telecom.	328674(28)	Electronic Engineering Materials & Components
5	Electronics & Telecom.	328675(28)	Computer Organization & Architecture
6	Electronics & Telecom.	328676(28)	Advanced Semiconductor Devices

*Note:*

1. 1/4<sup>th</sup> of total strength of students to minimum of twenty students is required to offer an elective in the college in a particular academic session
2. Choice of elective course once made for an examination cannot be changed in future examinations.

**Name of the Programme: Bachelor of Engineering    ::::    Duration of the Programme: Four Years**

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch:	<b>Electronics &amp; Telecommunication Engineering</b>	Semester:	<b>VI</b>		
Subject:	<b>Digital Signal Processing</b>	Code:	<b>328651(28)</b>		
Total Theory Periods:	<b>40</b>	Total Tutorial Periods:	<b>12</b>		
No. of class Tests to be conducted:	<b>2 (Minimum)</b>	No. of assignments to be submitted:	<b>2 (Minimum)</b>		
ESE Duration:	<b>Three Hours</b>	Maximum Marks in ESE:	<b>80</b>	Minimum Marks in ESE:	<b>28</b>

## Course objective:

- To study the basic mathematical techniques needed for analysis of discrete time signals and systems
- To study the various digital filter design techniques.
- To study the multirate digital signal processing techniques

## Course Outcomes:

At the end of this course students will demonstrate the ability to

1. Synthesize discrete time signals from analog signals.
2. Use time domain and frequency domain analysis tools.
3. Apply forward and reverse transformations.
4. Visualize various applications of DSP and explore further possibilities.
5. Design IIR and FIR filters.
6. Excel in H/W and S/W environment of Digital Signal Processing. .

## UNIT I Analysis of Discrete Time Signals and Systems:

Discrete Fourier analysis, Classification, Discrete Time Fourier Transform (DTFT) & its properties, Inverse DTFT. Discrete Fourier Transform (DFT) & its Properties, Inverse DFT. Fast Fourier Transform, Properties, Types of FFT, N-point Radix-2 FFT, Inverse FFT. Discrete Linear Convolution, Circular Convolution, Fast Convolution, Frequency Response of LTI system using Discrete Fourier Analysis. Discrete Cosine Transform.

**UNIT II Implementation of Discrete-time Systems:** Structures for the Realization of discrete-time systems, Structures for FIR systems: Direct, Cascade, Frequency Sampling & Lattice structures. Structures for IIR systems: Direct, Signal Flow Graphs & Transposed, Cascade, Parallel, Lattice & Lattice-Ladder structures. State space system analysis and structures.

**UNIT III FIR Filter Design:** Symmetric and Anti-symmetric FIR filters, FIR Filter design by window method (Rectangular, Bartlett, Hamming, Hanning, Blackman and Kaiser window), Frequency Sampling method, Optimum approximation of FIR filters, Design of FIR differentiators, Design of Hilbert transformers.

**UNIT IV IIR Filter Design:** Design of Discrete-time IIR filters from Continuous-time Filters: Filter design by Impulse invariant and bilinear transformation method: Butterworth, Chebyshev & Elliptic approximation Filter, Frequency transformation.

**UNIT V Multirate Digital Signal Processing:** Introduction, Decimation, Interpolation, Sampling rate conversion by rational factor, Filter design and implementation for sampling rate conversion: Direct form FIR digital filter structure, Polyphase filter structure, Time varying digital filter structure, Sampling rate conversion by an arbitrary factor.

## Name of Text Books:

1. Discrete Time Signal Processing by A.V. Oppenheim, R. W. Schaffer, & John R. Buck, , 2nd Edition, Prentice Hall, 1999. (Unit I, Unit II, Unit III, Unit IV)
2. Digital Signal Processing: Principles, Algorithms and Applications by John G. Proakis & D.G. Manolakis, Prentice Hall, 1997. (Unit II, Unit III, Unit IV, Unit V)
3. Digital Signal Processing by S. K. Mitra, 3rd edition, McGraw-Hill, 2007. (Unit V)

## Name of Reference Books:

1. Signals and Systems by A. V. Oppenheim, A. S. Willsky & S. H. NAWAB, 2nd edition, Prentice Hall, 1996.
2. Digital Signal Processing by S. Salivahanan, A. Vallavaraj, C. Gnanapriya, Tata McGraw-Hill, 2000.
3. Digital Signal Processing by A. Anand Kumar, PHI Learning Pvt. Ltd, 2012.

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch:	<b>Electronics &amp; Telecommunication Engineering</b>	Semester:	<b>VI</b>		
Subject:	<b>Electronic Circuit Design</b>	Code:	<b>328652(28)</b>		
Total Theory Periods:	<b>40</b>	Total Tutorial Periods:	<b>12</b>		
No. of class Tests to be conducted:	<b>2 (Minimum)</b>	No. of assignments to be submitted:	<b>2 (Minimum)</b>		
ESE Duration:	<b>Three Hours</b>	Maximum Marks in ESE:	<b>80</b>	Minimum Marks in ESE:	<b>28</b>

## Course objectives:

1. To become familiar with fundamental electronic circuits.
2. To learn to use common wave shaping Circuits.
3. To become familiar with Timer circuits designing for applications.
4. To be able to design active filter electronic circuits to perform realistic tasks.

## Course Outcome:

1. To understand electronics waveshaping circuits.
2. The student will be able to understand timer IC and Its Applications and Design concepts
3. Student will be able to understand Designing concepts of Active filters.

- UNIT I Signal Generators & Conditioners: Signal generators(op-amp):** Square Wave Generator, Triangular Wave Generator, Sawtooth Wave generator. Voltage sweep generator: General features of Time base signal, Exponential sweep circuit Current Sweep generator: A simple current sweep, Linearity correction through adjustment of driving waveform.  
**Signal conditioner:** Clipper Circuits (using diodes): Series Clipper, Parallel Clipper. Clamper Circuits (using Diodes): Negative Clamper, Positive Clamper. High Pass RC Circuit as Differentiator, Low Pass RC Circuit as Integrator.
- UNIT II Multivibrators:** Transistor as Switch, Types of Multivibrator (bistable, astable & monostable), Fixed and self biased binary , use of Commutating Capacitor, improving resolution, Schmitt trigger Emitter Coupled ,Monostable and Astable Multivibrator : Collector – Coupled and Emitter – Coupled Multivibrator.
- UNIT III Timer and its application:** 555 Timer, Functional Diagram, Monostable mode operation and its applications: missing pulse detector, Linear Ramp generator, Frequency Divider, Pulse Width modulation. Astable mode operation and its applications: FSK Generator, Pulse position modulator, Schmitt trigger.
- UNIT IV Principles of Active Filters:** Bilinear Transfer Function, Parts of  $T(j\omega)$ , Classification of Magnitude and Phase Response, Bode plots and Design. Cascading: Inverting and Non-inverting OP –AMP Circuits, Cascade Design, All pass Circuits: Phase shaping, Design parameters:  $\omega_0$  and Q, Biquad circuit and its frequency response.
- UNIT V Special Active Filters:** Design of Low –pass Butterworth Filters, Sallen and key Circuits, Resistive gain Enhancement, RC-CR Transformation, Design of Band – pass Butterworth Filters, Delyiannis-Friend Circuit, Stagger-Tuned Bandpass filter Design, Q Enhancement of the Friend circuit. Design of Low – pass and Band-pass Chebyshev Filters, Sensitivity concepts and their Application to Sallen and key Circuits.

## Name of Text Books:

1. Pulse, Digital and Switching Waveforms by Millman & Taub, TMH Publishing Co.(Unit-1,2)
2. Integrated Circuits: K. R. Botkar,9th Ed., Khanna Publications (Unit-3)
3. Analog Filter Design; Van –Valkenburg ; Holt –Standers International Edn. (Unit-4,5)

## Name of Reference Books:

1. Operational Amplifiers and Linear Integrated Circuits, Coughlin and Driscoll, 6th Ed., PHI
2. Linear Integrated Circuits, Roy Choudhury and Jain, 2nd Ed., New Age International Publishers.

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch:	<b>Electronics &amp; Telecommunication Engineering/Electronics &amp; Instrumentation/Applied Electronics &amp; Instrumentation</b>	Semester:	<b>VI</b>		
Subject:	<b>Microcontroller &amp; Embedded System</b>	Code:	<b>328653(28)</b>		
Total Theory Periods:	<b>40</b>	Total Tutorial Periods:	<b>12</b>		
No. of class Tests to be conducted:	<b>2 (Minimum)</b>	No. of assignments to be submitted:	<b>2 (Minimum)</b>		
ESE Duration:	<b>Three Hours</b>	Maximum Marks in ESE:	<b>80</b>	Minimum Marks in ESE:	<b>28</b>

## Course objectives:

- To make students familiar with the basic blocks of microcontroller device and Embedded system in general.
- To provide comprehensive knowledge of the architecture, features and interfacing with 8051 microcontroller.
- To use assembly and high level languages to interface the microcontrollers to various applications.

## Course Outcome:

1. To understand Microcontroller 8051 its architecture and its instruction set.
2. Gain knowledge about Counter/timer and interrupts in 8051 Microcontroller and Programming concepts.
3. Students will be able to do serial communication programming and gain knowledge of serial communication.
4. Students will be able to understand interfacing Microcontroller 8051 with devices.

- UNIT I Introduction to Microcontroller:** A brief History of Microcontrollers, Harvard Vs Von-Neumann Architecture; RISC Vs CISC, Classification of MCS-51 family based on their features ( 8051,8052, 8031, 8751, AT89C51 ), Pin configuration of 8051.  
**8051 Processor Architecture and Instruction Set:** Registers of 8051, Inbuilt RAM, Register banks, stack, on-chip and external program code memory ROM, power reset and clocking circuits, I/O port structure, Addressing modes, Instruction set and programming.
- UNIT II Counter/Timer and Interrupts of 8051:** Introduction, Registers of timer/counter, Different modes of timer/counter, Timer/counter programming, Interrupt Vs Polling, Types of interrupts and vector addresses, register used for interrupts initialization, programming of external interrupts, Timer interrupts.
- UNIT III Asynchronous Serial Communication and Programming:** Introduction to serial communication, Data Programming, RS232 standard, RS422 Standard, 1488 and 1489 standard, GPIB, Max 232/233 Driver.
- UNIT IV Interfacing with 8051:** Interfacing and programming of: ADC (0804,0808/0809,0848) & DAC (0808), stepper motor , 4x4 keyboard matrix, Relays, LED and Seven segment display, LCD, Interfacing (only) of different types of Memory , Address decoding techniques
- UNIT V Embedded Systems:** Introduction to an Embedded Systems, Defining the Embedded System, Real Life Examples of Embedded Systems, Characteristics of Real-Time Embedded Systems, Basics Of Developing For Embedded Systems, Embedded design challenges and development issues.

## Names of Text Books:

1. The 8051 Microcontroller and Embedded Systems using Assembly and C, Mazidi, Mazidi & McKinlay, 2nd Ed.,PHI.(Unit-I,II,III)
2. Embedded system, Frank Vahid.(Unit-IV)

## Names of Reference Books:

1. 8051 Programming, Interfacing and Applications K. J. Ayala, Penram Pub.
2. 8 bit Microcontrollers & Embedded Systems Manual.
3. Programming and Customizing the 8051 Microcontroller, Predko; TMH
4. Microcontrollers: Architecture, Programming, Interfacing and System Design, Rajkamal, Pearson Education.

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch:	<b>Electronics &amp; Telecommunication Engineering</b>	Semester:	<b>VI</b>		
Subject:	<b>VLSI Design</b>	Code:	<b>328654(28)</b>		
Total Theory Periods:	<b>40</b>	Total Tutorial Periods:	<b>12</b>		
No. of class Tests to be conducted:	<b>2 (Minimum)</b>	No. of assignments to be submitted:	<b>2 (Minimum)</b>		
ESE Duration:	<b>Three Hours</b>	Maximum Marks in ESE:	<b>80</b>	Minimum Marks in ESE:	<b>28</b>

## Course Objectives:

1. To understand the IC design aspects, basic fabrication steps.
2. To study the design rules & representation of circuits at lower level of abstraction.
3. To understand the layout design of few combinational and sequential circuits.
4. To study one of the HDL (hardware description language) for front end design.
5. To study internal structure of programmable logic devices.

## Course Outcomes:

1. Students are expected to understand CMOS fabrication details.
2. Students are expected to understand schematic, layout of combinational circuits.
3. Students are expected to understand schematic, layout of sequential circuits.
4. Students are expected to understand VHDL programming concepts.

<b>UNIT I</b>	<b>An Overview &amp; Analysis of CMOS Integrated Circuits:</b> Complexity and Design: Design Flow, VLSI Chip Types, Moore's Law; MOSFETs as Switch: FET Threshold Voltages, Pass Characteristics; Basic Logic Gates in CMOS: NOT Gate, NOR Gate, NAND Gate; Complex Logic Gates in CMOS: Structured Logic Design, XOR and XNOR Gates; Transmission Gate Circuits: Multiplexers, OR Gate, XOR/XNOR Gate. DC characteristics of the CMOS inverter, Switching Characteristics: Fall Time, Rise Time, Propagation Delay; Power Dissipation.
<b>UNIT II</b>	<b>Fabrication &amp; Physical Design of CMOS Integrated Circuits:</b> CMOS Layers; Designing FET Arrays; Basic Gate Designs; Complex Logic Gates; Euler Graph; Overview of Silicon Processing; Material Growth and Deposition; Lithography; CMOS Process Flow; CMOS Design Rules; Layout of Basic Structures: nWell, Active Areas, Doped Silicon Regions, MOSFETs, Active Contacts, Metal, Vias; Physical Design(Stick diagram &Layout Design) of Logic Gates: NOT, NAND & NOR.
<b>UNIT III</b>	<b>CMOS Subsystem Design:</b> Schematic and Layout of CMOS Combinational Circuits: Full adder circuit, Multiplexer, Parity Generator, Schematic and Layout of CMOS Sequential Circuits: SR Flip-Flop, JK Flip-Flop, & D Flip-Flop, 4x4 NOR based ROM Array, 4x4 NAND based ROM Array; Schematic of SRAM Schematic and operation of DRAM: 3-T DRAM 6-T DRAM;
<b>UNIT IV</b>	<b>Implementation Technology &amp; Introduction to VHDL:</b> Implementation Technology: CPLD Architecture, FPGA Architecture, LUT Design; Brief history of VHDL, Entity Declaration, Architecture Declaration, Modeling styles: Data Flow, Structural, Behavioral and Mixed Style. Assignment Statements, Select Signal Assignment, Conditional Signal Assignment, Component Declaration, Generate Statements, Concurrent and Sequential Assignment Statement, Process Statement, Case Statement. VHDL operators. VHDL programming of Multiplexer, Decoder, Encoder, Half Adder, Full Adder, 4-bit Adder, ALU.
<b>UNIT V</b>	<b>Sequential Logic Design using VHDL:</b> VHDL Programming for D-Latch, SR Flip-Flop, JK Flip-Flop, T Flip-Flop& D Flip-Flop, Shift Registers, Synchronous Counter: UP counter, Down counter, BCD counter; Moore Finite State Machine for Sequence Detector, MOD counter & Serial Adder. Mealy Finite State Machine for Sequence Detector, MOD counter & Serial Adder. Test Bench design for Half Adder, Full adder & D Flip-Flop.

## Textbooks:

1. Introduction to VLSI Circuits and Systems: John P. Uyemura, John Wiley & Sons (Unit-I & II).
2. CMOS Digital Integrated Circuits: Analysis & Design; Sung-Mo Kang & Yusuf Leblebici, TMH, (Unit-III)
3. Fundamentals of Digital Logic with VHDL Design, Brown, TMH Pub. (Uni- IV & V)
4. VHDL Primer by J. Bhaskar, PHI(Unit-IV & V)

## Reference Books:

1. CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Pearson Education Pub.
2. Basic VLSI Design by Pucknell&Esharghian,3rd Ed., PHI Pub.
3. CMOS circuit design, layout and simulation by Jacob Baker, PHI

**Name of the Programme: Bachelor of Engineering    ::::    Duration of the Programme: Four Years**

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch:	<b>Electronics &amp; Telecommunication Engineering</b>	Semester:	<b>VI</b>		
Subject:	<b>Information Theory &amp; Coding</b>	Code:	<b>328655(28)</b>		
Total Theory Periods:	<b>40</b>	Total Tutorial Periods:	<b>12</b>		
No. of class Tests to be conducted:	<b>2 (Minimum)</b>	No. of assignments to be submitted:	<b>2 (Minimum)</b>		
ESE Duration:	<b>Three Hours</b>	Maximum Marks in ESE:	<b>80</b>	Minimum Marks in ESE:	<b>28</b>

## Course objectives:

- To learn about various source coding and channel coding techniques.
- To study various error control coding techniques.
- To Gain knowledge about BCH code and implementation of RS encoder and decoder.
- To learn convolutional coding, viterbi decoding and turbo codes.
- To gain knowledge about Trellis Coded Modulation

## Course Outcomes:

1. Students will be able to understand the concept of various Source Coding Techniques and Channel Coding Techniques.
2. Students will be able to analysis various error control coding techniques.
3. Students will be able to understand BCH Code and RS Code.
4. Students will get the knowledge of convolutional Code.

<b>UNIT I</b>	<b>Source Coding and Channel Capacity Coding :</b> Introduction to Information Theory, Uncertainty and Information, Average Mutual Information and entropy, Information Measures for continuous Random Variables, Source Coding Theorem, Huffman coding, The Lempel-Ziv algorithm, Run Length Encoding and the PCX Format. Introduction to JPEG Standard for Lossless and Lossy Compression.(refer to text book) <b>Channel Capacity Coding:</b> Channel Models, Channel Capacity, Channel Coding, Information Capacity Theorem, The Shannon Limit.
<b>UNIT II</b>	<b>Error Control Coding (Channel Coding) Linear Block Codes for Error Correction &amp; Cyclic Codes:</b> Introduction to Error Correcting Codes, Basic Definitions, Matrix Description of Linear Block Codes, Equivalent Codes, Parity Check Matrix, Decoding of a Linear Block Code, Syndrome Decoding, Hamming Codes. <b>Cyclic Codes:</b> Polynomials, The Division algorithm for Polynomials, A Method for Generating Cyclic codes, Matrix Description of cyclic codes, Burst Error Correction.
<b>UNIT III</b>	<b>Bose-Chaudhuri Hocquenghem (BCH) Codes:</b> Introduction to BCH Codes, Primitive Elements, Minimal Polynomials, Generator Polynomials in Terms of Minimal Polynomials, some Examples of BCH Codes, Decoding of BCH Codes, Introduction to Reed-Solomon Codes,
<b>UNIT IV</b>	<b>Convolutional Codes:</b> Introduction to Convolutional Codes, Tree codes and Trellis Codes, Polynomial Description of Convolutional Codes (analytical Representation), distance Notions for Convolutional Codes, The Generating Function, Matrix Description of Convolutional Codes, Viterbi Decoding, Distance Bounds for Convolutional Codes.
<b>UNIT V</b>	<b>Trellis Coded Modulation:</b> Introduction to TCM, The Concept of Coded Modulation, Mapping by Set Partitioning, Ungerboeck's TCM Design Rules, TCM Decoder.

## Name of Text Books:

1. Information Theory coding & Cryptography by Rajan Bose,(Unit- I,II,III,IV,V) Tata McGraw-Hill,

## Name of Reference Books:

1. Principles of Digital Communication - Das Mullick Chatterjee, Willey Eastern Publications
2. Digital communication - Sklar, Pearson Publication
3. Digital communication - Prokakis, Tata McGrawHill

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch: **Electronics & Telecommunication Engineering**  
Subject: **Digital Signal Processing Laboratory**  
Total Lab Periods: **36**  
Maximum Marks: **40**

Semester: **VI**  
Code: **328661 (28)**  
Batch Size: **30**  
Minimum Marks: **20**

**List of Experiments:** *(At least Ten experiments are to be performed by each student)*

1. To generate the basic Analog and Discrete Signals.
2. Implementation of Linear convolution, Circular convolution, Linear convolution using circular convolution.
3. DFT Implementation for a given signal.
4. To plot Fourier Transform amplitude spectrum and phase spectrum for a given function .
5. To plot frequency response in Z-domain for the given transfer function.
6. To plot frequency response in S-domain for a given transfer function.
7. To plot Fast Fourier Transform (amplitude & phase).
8. To sample a sinusoidal signal at Nyquist rate, above the Nyquist Rate and below the Nyquist Rate.
9. Design & implementation of IIR filters [LPF, HPF, BPF, BSF].
10. Design & implementation of FIR filters [LPF, HPF, BPF, BSF].
11. To design various filters using Simulink.
12. To design a Graphical User Interface to display various basic signals [ sine wave , sinc wave, etc].
13. To perform Interpolation and decimation [ Multirate DSP].
14. To design a digital notch filter and embed it on a digital signal processor block.
15. Experiments with application of DSP in Communication/Speech Processing/Image Processing .

*(Institutes may append more programmes /Experiments based on the infrastructure available)*

## **List of Equipments/Machine Required:**

C++ Compiler, Simulation Software, DSP Processor kit, Digital Storage CRO, Spectrum Analyzer.

## **Recommended Books:**

1. Digital Signal Processing, Vallavaraj, Salivahanan, Gnanapriya, TMH
2. Stein, J. Digital Signal Processing - a computer science perspective. Wiley

# Chhattisgarh Swami Vivekanand Technical University, Bilai

Name of program	<b>Bachelor of Engineering</b>	
Branch:	<b>Electronics &amp; Telecommunication</b>	Semester: <b>VI</b>
Subject:	<b>Electronic Circuit Design Laboratory</b>	Code: <b>328662(28)</b>
Total Lab Periods:	<b>36</b>	Batch Size: <b>30</b>
Maximum Marks:	<b>40</b>	Minimum Marks: <b>20</b>

**List of Experiments:** *(At least Ten experiments are to be performed by each student)*

1. To design clipper circuits to clip positive, negative and also clipping at two independent levels.
2. To design Clamper circuits.
3. To design a Bistable multivibrator circuit and to draw its output waveform.
4. To design a Monostable multivibrator circuit and to draw its output waveform.
5. To design a Astable multivibrator circuit and to draw its output waveform.
6. To design an astable multivibrator using 555 timer
7. To design a monostable multivibrator using 555 timer.
8. To design a LPF using R & C and to study its characteristics
9. To design a HPF using R & C and to study its characteristics
10. To design a BPF using R & C and to study its characteristics
11. To design chebyshev filter using OPAMP and to plot its frequency response.
12. To design All Pass filter using OPAMP and to plot its frequency response.
13. To design Band-pass filter using OPAMP and to plot its frequency response.
14. To design HPF using OPAMP.
15. To design LPF using OPAMP.
16. To design HPF (Multistage) using OPAMP.

**List of Equipments/Machine Required:**

Discrete Components, Function Generator, Power Supply, CRO, AVO Meter, Multimeter, Voltmeter

**Recommended Books:**

Integrated Circuits: K. R. Botkar, Khanna Publishers.



# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Name of program	<b>Bachelor of Engineering</b>	Semester:	<b>VI</b>
Branch:	<b>Electronics &amp; Telecommunication</b>	Code:	<b>328663(28)</b>
Subject:	<b>Microcontroller &amp; Embedded System Laboratory</b>	Batch Size:	<b>30</b>
Total Lab Periods:	<b>36</b>	Minimum Marks:	<b>20</b>
Maximum Marks:	<b>40</b>		

**List of Experiments:** *(At least Ten experiments are to be performed by each student)*

1. Write a microcontroller 8051 program to transfer the bytes into RAM locations starting at 50H, assuming that ROM space starting at 240H contains CHHATTISGARH by using – a) Counter, b) nullchar. for end of string .
2. Write a microcontroller 8051 program to get hex data on the range of 00-FFh from port 0 and convert it to decimal. Save the digits in R7, R6 and R5, where the least significant digit is in R7.
3. Write a microcontroller 8051 program to add two 16 Bit unsigned numbers. Operands are two RAM variables. Results to be in R1-R0 pair.
4. Write a microcontroller 8051 program to subtract an unsigned 16 Bit number from another. Operands are two RAM variables. Results to be in R1-R0 pair.
5. Write a microcontroller 8051 program to add two unsigned 32-bit numbers. Operands are two RAM variables. Results to be in R1-R0 pair.
6. Write a microcontroller 8051 program to add two 16 Bit signed numbers.
7. Write a microcontroller 8051 program to convert a binary number to equivalent BCD
8. Write a microcontroller 8051 program to convert a packed BCD number to two ASCII numbers and place them in R5 and R6.
9. Write a microcontroller 8051 program to calculate the square root of an 8-bit number using iterative method.
10. Write a microcontroller 8051 program that generates 2kHz square wave on pin P1.0, 2.5 kHz on pin P1.2 and 25 Hz on pin P1.3.
11. Write a microcontroller 8051 program for counter 1 in mode 2 to count the pulses and display the state of the TL1 count on P2. Assume that the clock pulses are fed to pin T1.
12. Write a microcontroller 8051 program to transfer letter “N” serially at 9600 baud, continuously. Assume crystal frequency to be 11.0592 MHz.
13. Write a microcontroller 8051 program to transfer word “CSVTU” serially at 4800 baud and one stop bit, continuously. Assume crystal frequency to be 11.0592 MHz.
14. Write a microcontroller 8051 program to receive bytes of data serially, and put them in P1. Set the baud rate at 2400 baud, 8-bit data, and 1 stop bit. Assume crystal frequency to be 11.0592 MHz.

**List of Equipments/Machine Required:**

Microcontroller kit, Interfacing kit, Keyboard, Monitor, SMPS for Microcontroller

# Chhattisgarh Swami Vivekanand Technical University, Bilai

Name of program	<b>Bachelor of Engineering</b>	Semester:	<b>VI</b>
Branch:	<b>Electronics &amp; Telecommunication</b>	Code:	<b>328664(28)</b>
Subject:	<b>VLSI Design Laboratory</b>	Batch Size:	<b>30</b>
Total Lab Periods:	<b>36</b>	Minimum Marks:	<b>20</b>
Maximum Marks:	<b>40</b>		

**List of Experiments:** *(At least Ten experiments are to be performed by each student)*

1. To Study Architecture of CPLD
2. To Study Architecture of FPGA
3. To Design Half Adder in Data Flow Style of Modeling and Implement it in the CPLD.
4. To Design Full Adder in Structural Style of Modeling and Implement it in the FPGA.
5. To Design 4:1 Multiplexer in Behavioral Modeling and Implementation in CPLD.
6. To Design 16:1 Multiplexer using Generate statement and Implementation in FPGA.
7. To Design 8bit adder using Generic statement and Implementation in CPLD.
8. To Design D Flip-Flop in Behavioral Modeling.
9. To Design Sequence Detector using Moore Machine in Behavioral Modeling.
10. To Design Serial Adder using Mealy Machine in Behavioral Modeling.
11. To Prepare and Verify the Layout for NOT Gate.
12. To Prepare and Verify the Layout for NAND Gate.
13. To Prepare and Verify the Layout for NOR Gate.
14. To Prepare the Layout for D-FF.
15. To Prepare the Layout for the logic equation  $(a * (b+c))'$

**EDA Tools to be used:**

**Front End:** Modelsim, FPGA Advantage, Xilinx, EdWinXP, ActiveHDL.

**Back End:** Cadence, Zeni-EDA, Calibre, Tanner, Synopsys, H-Spice

**CPLD:** XC9572, XC95108. **FPGA:** XC3S400

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Name of Program:	<b>Bachelor of Engineering</b>	Semester:	<b>VI</b>
Branch:	<b>Common to All Branches</b>	Code:	<b>300665 (76)</b>
Subject:	<b>Managerial Skills</b>	Tutorial Period:	<b>NIL</b>
No. of Lectures:	<b>2/Week</b>	Marks in TA:	<b>40</b>
Total Marks in ESE:	<b>NIL</b>	Minimum number of Class Tests to be conducted:	<b>Two</b>

## Objective:

The course is introduced to develop managerial skills tremendously and enrich the abilities to enable one to meet the challenges associated with different job levels. Managerial skills are essential for overall professional development of an individual apart from gaining technical knowledge in the subject.

## Course Objectives

Upon completion of this course, the student shall be able

- To define and explain the concept of managerial, written and oral communication skill;
- To understand the leadership skill;
- To develop self-appraisal and understand distinction between leader and manager;
- To develop positive attitude and thinking; and
- To understand managerial functions and develop creativity.

**UNIT I Managerial Communication Skills:** Importance of Business Writing: writing business letters, memorandum, minutes, and reports- informal and formal, legal aspects of business communication, oral communication- presentation, conversation skills, negotiations, and listening skills, how to structure speech and presentation, body language.

**UNIT II Managerial skills - Leadership:** Characteristics of leader, how to develop leadership; ethics and values of leadership, leaders who make difference, conduct of meetings, small group communications and Brain storming, Decision making, How to make right decision, Conflicts and cooperation, Dissatisfaction: Making them productive.

**UNIT III Proactive Manager:** How to become the real you: The journey of self-discovery, the path of self-discovery, Assertiveness: A skill to develop, Hero or developer, Difference between manager and leader, Managerial skill check list, team development, How to teach and train, time management, Stress management, Self-assessment.

**UNIT IV Attitudinal Change:** Concept of attitude through example, benefits of right attitude, how to develop habit of positive thinking, what is fear? How to win it? How to win over failure? How to overcome criticism? How to become real you? How to Motivate? How to build up self confidence?

**UNIT V Creativity:** Creativity as a managerial skill, Trying to get a grip on creativity. Overview of Management Concepts: Function of Management: Planning, organizing, staffing, controlling.

## Course Outcome

- The students will be able to develop formal and informal, negotiation, written and oral communication skill;
- The students will be able to develop manage groups, resolve conflicts and leadership skill and decision making qualities;
- The students will be able to develop self-appraisal, teaching, training and managing stress and time;
- The students will be able develop positive thinking, motivating team members and winning race; and
- The students will be able to develop creativity and fundamental management functions.

## Text Books:

1. Basic Managerial Skills for all by E.H. Mc Grawth, Prentice Hall India Pvt Ltd,2006
2. Basic Employability Skills by P. B. Deshmukh, BSP Books Pvt. Ltd., Hyderabad, 2014

## Reference Books:

1. How to develop a pleasing personality by Atul John Rego, Better yourself books, Mumbai,2006
2. The powerful Personality by Dr. Ujjawal Patni & Dr. Pratap Deshmukh, Fusion Books, 2006
3. How to Success by Brian Adams, Better Yourself books, Mumbai, 1969

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch: **Electronics & Telecommunication Engineering**  
Subject: **Internet & Web Technology**  
(Professional Elective – I)

Semester: **VI**  
Code: **328671(28)**

Total Theory Periods: **40**  
No. of class Tests to be conducted: **2 (Minimum)**

Total Tutorial Periods: **NIL**  
No. of assignments to be submitted: **2 (Minimum)**

ESE Duration: **Three Hours**

Maximum Marks in ESE: **80** Minimum Marks in ESE: **28**

## Course objective:

1. To provide the fundamental concepts of Internet and to make students recognize the difference between various Internet protocols.
2. To introduce the concept of e-mail, list server & file transfer protocols.
3. To introduce the concept of HTML, Javascript & XML.
4. To introduce the concept of Internet security, Firewalls, E-commerce & EDI.

## Course Outcome:

1. Students will be familiar with various Internet protocols and the concepts of Internet.
2. Students will be able to differentiate between various e-mail protocols and their working.
3. Students will be familiar with the concept of remote login with the understandability of hosting and maintaining of website.
4. Students will also get knowledge about Internet security and Firewalls.

- UNIT I INTRODUCTION TO INTERNET:** Introduction, Evolution of Internet, Internet Applications, Internet Protocol -TCP/IP, UDP, HTTP, Secure Http(Shttp), Internet Addressing – Addressing Scheme – Ipv4 & IPv6, Network Byte Order, Domain, Name Server and IP Addresses, Mapping. Internet Service Providers, Types Of Connectivity Such as Dial-Up Leaded Vsat. Web Technologies: Three Tier Web Based Architecture; Jsp, Asp, J2ee, Net Systems.
- UNIT II HTML CSS AND SCRIPTING:** HTML - Introduction, Sgml, Dtd(Document Type Definition, Basic Html Elements, Tags and usages, HTML Standards , Issues in HTML Dhtml: Introduction Cascading Style Sheets: Syntax ,Class Selector, Id Selector Dom (Document Object Model) & Dso (Data SourceObject) Approaches To Dynamic Pages: Cgi, Java Applets, Plug Ins, Active X, Java Script – Java Script Object Model, Variables-Constant – Expressions, Conditions-Relational Operators- Data Types – FlowControl – Functions & Objects-events and event handlers – Data type Conversion & Equality – Accessing HTML form elements.
- UNIT III XML:** What is XML – Basic Standards, Schema Standards, Linking & Presentation Standards, Standards that build on XML, Generating XML data, Writing a simple XML File, Creating a Document type definition, Documents & Data ,Defining Attributes & Entities in the DTD ,Defining Parameter Entities & conditional Sections, Resolving a naming conflict, Using Namespaces, Designing an XML data structure,Normalizing Data, Normalizing DTDS.
- UNIT IV INTERNET SECURITY & FIREWALLS:** Security Threats From Mobile Codes, Types Of Viruses, Client Server Security Threats,Data & Message Security, Various electronic payment systems,Introduction to EDI, Challenges–Response System, Encrypted Documents And Emails , Firewalls:Hardened Firewall Hosts, Ip- Packet Screening, Proxy Application Gateways, Aaa (Authentication ,Authorization and Accounting).
- UNIT V WEBSITE PLANNING & HOSTING:** Introduction, Web Page Lay-Outing, Where To Host Site, Maintenance Of Site, Registration Of Site On Search Engines And Indexes, Introduction To File Transfer Protocol, Public Domain Software, Types Of Ftp Servers (Including Anonymous), Ftp Clients Common Command. Telnet Protocol, Server Domain, Telnet Client, Terminal Emulation. Usenet And Internet Relay Chat

## Text Books:

1. Internet & Intranet Engineering,- Daniel Minoli, TMH.
2. Alexis Leon and Mathews Leon – Internet for Every One, Tech World.

## Reference Books:

1. Eric Ladd, Jim O'Donnel –“Using HTML 4, XML and JAVA”-Prentice Hall of India - 1999.
2. Beginning Java Script– Paul Wilton – SPD Publications –2001.
3. Frontiers of Electronics of Commerce, Ravi kalakota & Andrew B. Whinston, Addison Wesley.

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch:	<b>Electronics &amp; Telecommunication Engineering</b>	Semester:	<b>VI</b>
Subject:	<b>Operating System (Professional Elective – I)</b>	Code:	<b>328672(28)</b>
Total Theory Periods:	<b>40</b>	Total Tutorial Periods:	<b>NIL</b>
No. of class Tests to be conducted:	<b>2 (Minimum)</b>	No. of assignments to be submitted:	<b>2 (Minimum)</b>
ESE Duration:	<b>Three Hours</b>	Maximum Marks in ESE:	<b>80</b>
		Minimum Marks in ESE:	<b>28</b>

## Course objective:

1. To provide an understanding of the functions of operating systems.
2. To provide an insight into internals and functional modules of operating systems.
3. To study the concepts underlying the design and implementation of memory management of operating systems.
4. To make student able to understand deadlocks and to recover them.
5. To make student understand the core structure, functions and design principles of distributed operating system will be introduced with this subject.

## Course Outcome:

1. The student will be able to learn the various functionalities of OS.
2. The student will be able to use the various algorithms and techniques to perform the various jobs performed by operating systems
3. The student will be able to get the overview of how operating system is designed.
4. The student will be able to demonstrate how various resources are managed by operating system

- UNIT I Introduction to operating system:** Functions provided by operating system, Introduction to multi programming, Time sharing and real time systems, Introduction to file systems, Access and allocation methods of file systems, Directory structure of a file system on a disk and tape, File protection.
- UNIT II Introduction to scheduling:** Process concept, states of process, Process control block, CPU scheduling, various types of CPU scheduling algorithms and their evaluation. Meaning of disk and drum scheduling, Various types of disk and drum scheduling algorithms like FCFS, SCAN etc., CPU protection.
- UNIT III Introduction to memory management:** Various types of memory management schemes like paging, Segmentation etc. Concept of virtual memory, demand paging, Various page replacement algorithms, thrashing and methods to tackle it, Memory protection.
- UNIT IV Concurrency and Deadlock:** Meaning of deadlocks, Resource allocation graphs, Deadlock Characterization, Various methods to avoid deadlocks like deadlock avoidance, Deadlock detection, Deadlock prevention, Banker's algorithm for deadlock avoidance. Introduction to concurrent processing, Precedence graphs, Critical section problem, Semaphore concept, Study of classical process co-ordination problem.
- UNIT V Introduction to distributed systems:** I/O Subsystem Principles of I/O Hardware: I/O devices, device controllers, direct memory access. Principles of I/O Software: Goals, interrupt handlers, device drivers, device independent I/O Software. User space I/O software, I/O protection. Distributed file systems: Design, Implementation, and trends. Performance Measurement: Important trends affecting performance issues, performance measures, evaluation techniques, bottlenecks and saturation feedback loops. Case study of UNIX and DOS operating systems.

## Text Books:

1. Operating System Concepts, James L. Peterson and Abraham Silberschatz (Addison-Wesley)
2. Modern Operating System, Andrew .S. Tanenbaum, PHI

## Reference Books:

1. Operating System Concepts & Design, Milan Milenkovic (MGH)
2. An Introduction to Operating Systems, Harvey M. Dietel(Addison Wesley)

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch:	<b>Electronics &amp; Telecommunication Engineering</b>	Semester:	<b>VI</b>		
Subject:	<b>Biomedical Electronics (Professional Elective – I)</b>	Code:	<b>328673(28)</b>		
Total Theory Periods:	<b>40</b>	Total Tutorial Periods:	<b>NIL</b>		
No. of class Tests to be conducted:	<b>2 (Minimum)</b>	No. of assignments to be submitted:	<b>2 (Minimum)</b>		
ESE Duration:	<b>Three Hours</b>	Maximum Marks in ESE:	<b>80</b>	Minimum Marks in ESE:	<b>28</b>

## Course objective:

1. To provide an understanding the function of Man Instrument System.
2. To provide an understanding of the heart and cardiovascular system and measurement of parameters involved.
3. To know the methods of measurements of various Biological parameters.
4. To make student understand the devices used and medical equipment used in patient-care and monitoring.
5. To know about Biotelemetry and its application in patient care.

## Course Outcome:

1. Student will be able to understand problem found un measuring a living system.
2. Student will get an idea of Bio-electric potentials in cardio vascular system
3. Student will be able to understand measurement of Biological Parameters..
4. Student will be able to understand. Application of Telemetry and various equipment used in patient care.

- UNIT I Man Instrument System and Sources of Bio-potentials :** Introduction to Man-Instrument System, Components of Man-Instrument System, Physiological System of the Body, Problems Encountered in Measuring a Living System, Sources of Bio-electric Potentials: Action and Resting Potentials, ECG, EEG, EMG and their characteristics.
- UNIT II Bio Electric Potential Measurements:** Bio potential Electrodes: Electrode theory, Microelectrodes, surface electrodes and needle electrodes, Cardiovascular Measurements: The Heart and Cardiovascular System, Electrical activity of heart, Electrocardiography.
- UNIT III Measurements of Biological Parameters:** Measurement of Blood Pressure and Flow, Plethysmography, Measurement of Heart Sound, Measurement of Temperature, Ultrasonic Diagnosis.
- UNIT IV Patient Care and Monitoring:** The Elements of Intensive Care Monitoring, Pacemakers, Defibrillators, Heart Lung Machine, CT scan system, MRI scan system, Electrical Safety of Medical Equipment.
- UNIT V Biotelemetry:** Introduction, Physiological parameters Adaptable to Biotelemetry, The components of a Biotelemetry System, Implantable Units, Applications of Telemetry in Patient care, use of Lasers, Recent advances in Biomedical Instrumentation.

## Name of Text Books:

1. Biomedical Instrumentation & Measurement by L. Cromwell, F.J. Weibell and E.A. Pfeiffer, 2nd Ed., PHI
2. Principles of Medical Electronics & Biomedical Instrumentation, C Raja Rao & S.K Guha, University Press

## Name of Reference Books:

1. Electronics in Medicine and Biomedical Instrumentation – Nandini K. Jog, PHI
2. Biomedical Instrumentation – Dr. A. Arumugam, Anuradha Agencies, Chennai.
3. Handbook of Biomedical Instrumentation by R.S. Khandpur, TMH Pub. Co.
4. Introduction to Biomedical Engineering, Domach, Pearson Education

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch:	<b>Electronics &amp; Telecommunication Engineering</b>	Semester:	<b>VI</b>		
Subject:	<b>Electronic Engineering Materials &amp; Components (Professional Elective – I)</b>	Code:	<b>328674(28)</b>		
Total Theory Periods:	<b>40</b>	Total Tutorial Periods:	<b>NIL</b>		
No. of class Tests to be conducted:	<b>2 (Minimum)</b>	No. of assignments to be submitted:	<b>2 (Minimum)</b>		
ESE Duration:	<b>Three Hours</b>	Maximum Marks in ESE:	<b>80</b>	Minimum Marks in ESE:	<b>28</b>

## Course objective:

1. To study the fabrication process of monolithic ICs.
2. To study the dielectric and magnetic property of materials.
3. To understand the characteristics of various components.

## Course Outcome:

1. Student will be able to understand the fabrication process of Diodes and Transistors.
2. Student will be able to understand the properties of materials used in semiconductor devices.

- UNIT I Monolithic Techniques:** The basic fabrication sequence; Growth and refining of silicon crystals; Epitaxial process; Diffusion; Diffusion system; Surface passivation; Photolithography; Metallization; Isolation; Crossovers. Monolithic Transistors and diodes; Monolithic junction FET and MOSFET; Integrated resistors; Junction Capacitors. MOS ICs; The silicon –gate and silicon-nitride MOS structure; Advantages and limitations of MOS devices; Charge coupled devices.
- UNIT II Dielectric Properties of Insulators:** Static Field; static Dielectric Constant; Polarization; Dielectric Constant of Monatomic gases; Dielectric constant of solids. Properties of Ferro electric materials; Spontaneous polarization Piezo Electricity, Alternating fields; Electronic and Ionic Polarizability-Frequency Dependence; Complex Dielectric Constant of Non-Dipolar Solids; Dipolar Relaxation and Dielectric Losses.
- UNIT III Magnetic Properties of Materials:** Summary of Concepts pertaining to Magnetic Fields; Magnetic Dipole moment of a Current Loop; Magnetization from a Macroscopic Point of View; Orbital Magnetic Dipole Moment and Angular Moment of Two Simple Atomic Models; Lenz's: Induced Dipole Moment Classification of Magnetic Materials: Diamagnetism: Origin of Permanent Magnetic Dipole in matter: Paramagnetic Spin System: Properties of Ferromagnetic Materials: Spontaneous Magnetization and Curie- Weiss Law; Ferromagnetic Domains and Coercive Forces; Anti Ferromagnetic and Ferrimagnetic Materials.
- UNIT IV Conduction in Metals:** Ohm's Law; Relaxation; Collision Time and Mean Free Path; Electron Scattering and Receptivity of Metals; Heat Developed in Current Carrying Conductors; Thermal Conductivity of Metals.
- UNIT V Components:** Resistances: Resistive Elements: Terminals and Protective Means: Characteristics of Resistor: Characteristics of Different Capacitors and Their Selection Factors: Variable Capacitors: Precision Variable Capacitors: General Purpose Variable Capacitors: Trimmers: Characteristics of Electronics power Transformers and Audio Transformers: Design Consideration: Low and High Frequency Equivalent Circuits of Audio Transformers; High Frequency Equivalent Circuits of Components.

## Name of Text Books:

1. Electronic Engineering Materials and Devices – John Allison, TMH
2. Electrical Engineering Materials – A.J. Dekker, PHI.
3. A Monograph on Electronics Design Principles: N.C. Goyal and R.K. Khetan: Khanna Publishers: (For Unit - V).

## Name of Reference Books:

1. Integrated Electronics – Millmann & Halkias, TMH
2. Structure and Properties of Materials Vol IV : Robert M Rose. Lawrence A Shepard and John Wulf: Wiley Eastern.
3. Electrical Engineering Materials – S.P. Seth & P.V. Gupta, Dhanpat Rai Publications.

# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch:	<b>Electronics &amp; Telecommunication Engineering</b>	Semester:	<b>VI</b>
Subject:	<b>Computer Organization &amp; Architecture (Professional Elective – I)</b>	Code:	<b>328675(28)</b>
Total Theory Periods:	<b>40</b>	Total Tutorial Periods:	<b>NIL</b>
No. of class Tests to be conducted:	<b>2 (Minimum)</b>	No. of assignments to be submitted:	<b>2 (Minimum)</b>
ESE Duration:	<b>Three Hours</b>	Maximum Marks in ESE:	<b>80</b>
		Minimum Marks in ESE:	<b>28</b>

## Course objective:

1. To know about Central processor organization.
2. To know about Control unit organization.
3. To provide an Insight into Arithmetic processor design.
4. To provide an insight into Input/Output organization & Memory organization.

## Course Outcome:

1. Student will be able to understand Central processor organization.
2. Student will be able to understand Instruction set and micro programming.
3. Student will be able to understand Algorithm in arithmetic control unit.
4. Student will be able to understand Input/output and memory organization.

- UNIT I**     **Central Processor organization:** Bus organized computer, Memory address structure, Memory data register, program counter, Accumulator, Instruction register, Program counter, Accumulator, Instruction register, Instruction field, Micro operations, Register transfer languages, Instruction field, Decoding and execution, Instruction formats and addressing modes.
- UNIT II**     **Control unit organization:** Instruction sequencing, Instruction interpretation, Hardwired control, Micro-programmed control organization, Control memory, Address sequencing, Micro-instruction, Formats, Micro-program sequence, Microprogramming.
- UNIT III**     **Arithmetic processor design:** Addition and subtractions algorithm, Multiplication algorithm, Division algorithm Processor configuration, Design of control unit and floating point arithmetic.
- UNIT IV**     **Input Output organization:** Programmed I/O., I/O, addressing, I/O instruction, Synchronization, I/O interfacing, Interrupt mechanism, DMA, I/O processors and data communication, RISC, CISC, Loosely Coupled & Tights Coupled system.
- UNIT V**     **Memory organization and multiprocessing:** Basic concepts and terminology, Memory hierarchy, Semiconductor memories (RAM, ROM), Multiple module, Memories and interleaving (Virtual memory, Cache memory, Associative memory), Memory management hardware requirements, RISC & CISE Processor.

## Name of Text Books:

1. Computer System Architecture by M. Morris Mano, PHI
2. Computer Organization Architecture by J.P. Hayes, PHI

## Name of Reference Books:

1. Digital Computer Logic Design By M. Morris Mano, PHI
2. Structured Computer Organization by Andrew S. Tanenbaum PHI
3. Computer Organisation and Design, Pal-Chauduri, PHI



# Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch:	<b>Electronics &amp; Telecommunication Engineering</b>	Semester:	<b>VI</b>		
Subject:	<b>Advanced Semiconductor Devices (Professional Elective – I)</b>	Code:	<b>328676(28)</b>		
Total Theory Periods:	<b>40</b>	Total Tutorial Periods:	<b>NIL</b>		
No. of class Tests to be conducted:	<b>2 (Minimum)</b>	No. of assignments to be submitted:	<b>2 (Minimum)</b>		
ESE Duration:	<b>Three Hours</b>	Maximum Marks in ESE:	<b>80</b>	Minimum Marks in ESE:	<b>28</b>

## Course objective:

1. To study the concepts of metal Semiconductor devices.
2. To understand concept of Tunnelling study tunnel devices.
3. To introduce concept of Transferred electron effect and Study various modes of such devices.
4. To study about advanced MOS Devices.

## Course Outcome:

1. Student will be able to understand concepts of MESFET, CCDS.
2. Student will be able to understand concepts of tunneling.
3. Student will be able to understand Transferred-Electron devices.
4. Student gets an idea of MOSFET devices.

- UNIT I Metal Semiconductor Devices:** Metal-vacuum boundary: Schottky effect, Metal-Semiconductor boundary: Ohmic contact, Current transport across a metal-semiconductor boundary, Metal-Insulator-Semiconductor (MIS) System, Metal-Semiconductor-Field Effect-Transistor (MESFET), Charge Coupled Devices (CCDs)
- UNIT II Semiconductor Tunnel Devices:** Tunneling from the point of view of quantum measurement, Analysis of the Tunneling effect; Tunneling probability, Tunneling current density, Resonant tunneling. Tunnel Diodes; Qualitative and quantitative explanation of the Tunnel Diode I-V characteristics, Tunneling in a resonant tunneling diode, Indirect tunneling, Excess current, Thermal current in a tunnel diode, Dependence of tunnel diode characteristics on various parameters.
- UNIT III Transferred – Electron Devices:** Introduction, Transferred – Electron effect; Bulk Electron Negative Differential Resistivity, Modes of Operation; Ideal – Uniform Field mode, Accumulation Layer Mode, Transit Time Dipole Layer Mode, Quenched Dipole Layer Mode, Limited Space Charge Accumulated Mode. Device performances; Cathode Contacts, Power-Frequency Performance and Noise, Functional Devices.
- UNIT IV MOSFET:** Introduction, Basic Device Characteristics; Non-equilibrium condition, Linear and Saturation regions, Sub threshold region, Non-uniform Doping and Buried Channel Devices, Short-Channel Effects, MOSFET Structures; Scaled Down devices, HMOS, DMOS, Recessed-Channel MOSFET, Schottky-Barrier Source and Drain, Thin Film Transistor, SOI, VMOS, HEXFET.
- UNIT V Transistor Structures:** Electron Transport in short devices and Compound Semiconductor Technology, Permeable Base Transistors, Planar Doped Barrier Devices, Real Space Transfer and Hot Electron Injection Transistors, Superlattice Devices.

## Name of Text Books:

1. Physics of Semiconductor Devices, S.M Sze, Wiley Student Edition
2. Physics of Semiconductor Devices, Michael Shur, PHI

## Name of Reference Books:

1. Physics of Semiconductor Devices, Dilip K. Roy, University Press
2. Semiconductor Devices-Modelling & Technology, Nandita Dasgupta & Amitava Dasgupta, PHI

**Name of the Programme: Bachelor of Engineering    ::::    Duration of the Programme: Four Years**