RCET, BHILAI

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Scheme of teaching and examination

M.Tech. (DIGITAL ELECTRONICS) in the Department of Electronics & Telecommunication

Ist SEMESTER

S.No	Board of Study	Subject Code	Subject Name	Periods per week			Scheme of Exam			Total Marks	Credit L+(T+P)/2
							Theory/Practical				
				L	T	P	ESE	CT	TA		
1	Electronics & Telecom.	555111 (28)	Advance Digital Signal Processing	3	1	-	100	20	20	140	4
2	Electronics & Telecom.	555112 (28)	Advanced Microprocessors & Interfaces	3	1	-	100	20	20	140	4
3	Electronics & Telecom.	555113 (28)	Digital Communication Techniques	3	1	-	100	20	20	140	4
4	Electronics & Telecom.	555114 (28)	VLSI Design	3	1	-	100	20	20	140	4
5	Refer Table – I		ELECTIVE –I		1	-	100	20	20	140	4
6	Electronics & Telecom.	555121 (28)	Advanced Digital Signal Processing Lab	--	-	3	75	--	75	150	2
7	Electronics & Telecom.	555122 (28)	Advanced Microprocessors & Interfaces Lab	-	-	3	75	--	75	150	2
TOTAL				**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

L-Lecture, T- Tutorial, P- Practical, ESE- End Semester Examination, CT- Class Test,TA- Teacher's Assessment

Note : Duration of all theory papers will be of Three Hours.

Table – I		
Elective – I		
Board of Study	**Code**	**Subject**
Electronics & Telecom.	555131 (28)	Fiber Optic Networks
Electronics & Telecom.	555132 (28)	Reliability Engineering
Electronics & Telecom.	555133 (28)	Parallel Processors
Electronics & Telecom.	555134 (28)	Digital Instrumentation

Note (1) – 1/4th of total strength of students subject to minimum of twenty students is required to offer an elective in the college in a Particular academic session .

Note (2) – Choice of elective course once made for an examination cannot be changed in future examinations.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. I Sem.** Branch: **Electronics Telecom.**
Subject: **Advance Digital Signal Processing** Code: **555111 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: 02

Unit - I
Frequency domain representation of Discrete signals: Discrete time Fourier transform (DTFT), Inverse DTFT, Properties of DTFT, Discrete Fourier Transform (DFT), Properties of DFT, IDFT, Twiddle factor, DFT & IDFT using matrix method, circular convolution, Analytical, Graphical and Matrix method for circular convolution, Fast convolution, Fast Fourier transform (FFT), Radix – 2 FFT, DIT-FFT, DIT-IFFT, DIF-FFT, Radix –2 DIF – IFFT, Composite radix FFT, Applications of FFT.

Unit - II
Implementation of discrete-time systems: Block diagram and signal flow graph representation of IIR and FIR filters, Realization of IIR filters Direct –I, Direct-II, Cascade, Parallel, Ladder and Transposed Realization), Realization of FIR filters (Direct, Cascade and linear phase FIR structure). Design of digital filter, specification of FIR filters, General consideration, design of FIR filters, Symmetric and antisymemmetric FIR filter, Design of FIR filter using Windows, Frequency sampling method, Hilbert Transformers.

Unit - III
Filter Design Techniques: Design of DTIIR filters. From continuous time filters, Introduction to analog filters for designing Digital filters (Butter worth and chebyshev filters), filters design using Impulse invariant, Bilinear Z transform, Matched Z-Transform and Approximation of derivatives methods, frequency transformation, Frequency Transformations, Design of IIR Filters in frequency Domain, Difference between FIR and IIR filters.

Unit - IV
Real time DSP Systems: Real time DSP systems: DSP and its benefits, key DSP operations, Typical Real time DSP system, ADC process, Uniform and Nonuniform quantization and Encoding DAC Process, Signal recovery, sampling of low pass and Band pass signals, Digital signal processors, Evaluation boards for real time signal processing, Multirate Digital Signal Processing, Decimation by factor D, Interpolation by factor I, Filter and implementation for sampling rate conversion, multistage implementation of sampling rate conversion, sampling rate conversion of band pass signals, Application of Multirate signal processing.

Unit - V
Issues involved in DSP processor design, Architecture and applications of TMS 320 C6XX, Multiprocessing with DSP processors, Applications of DSP to speech & radar signal processing, Adaptive removal of ocular artifacts from human EEGs.

***Text Books**:*

1. Advanced Digital Signal Processing, Proakis, McMillan
2. Ifeachor Emmanuel C. and Barrie W. Jervis, “Digital Signal Processing A Practical Approach” Pearson Education Ltd., Fifth Indian Reprint, 2005.

Reference Books:

1. Jhonson Jonny, “Digital Signal Processing”, Tata Mc Graw Hill Publication.
2. Schafer R.W. and A.V. Oppeheim, “Digital Signal Processing”, Prentice Hall of India, New Delhi, 1999
3. Kue R., “Introduction to Digital Signal Processing”, Mc Graw Hill, New York 1988.
4. Porat B., “A course in DSP John Wiley & Sons, Inc., New York, 1997.
5. Bose N.K. “Digital Filters: Theory & Application” Elsevier, New York, 1995.
6. Proakis J.G. and D.G. Manolakis, “Digital Signal Processing”, Prentice Hall of India, New Delhi, 1999
7. Adaptive Filter Theory, Simon Haykin Jhon Wiley
8. Theory and Applications of Digital Signal Processing by Rabiner & Gold, Prentice -Hall.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. I Sem.** Branch: **Electronics &Telecom.**
Subject: **Advanced Microprocessors & Interfaces** Code: **555112 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: 02

UNIT – I

Architecture 16 bit microprocessors: Intel 8086 Architecture- Memory address space and data organization - Segment registers and memory segmentation - I/O address space - Addressing modes - Comparison of 8086 and 8088 - Basic 8086/8088 configuration - Minimum mode - Maximum mode - System timing. Bus interface. Interrupts and interrupt priority management. Intel 80286 Architecture- Comparison with 8086 processor.

UNIT – II

Architecture of 32 bit Microprocessors: Intel 80386 Architecture Special 80386 Registers- Memory management - interrupts and exceptions - management of tasks - Real, protected and virtual 8086 mode- Introduction to 80486 microprocessor Architecture Comparison with 80386 processor.

UNIT – III

Advanced Microprocessors: Introduction to Pentium and Pentium pro architectures: RISC concepts- BUS operation- Super scalar architecture- Pipelining-Branch prediction-Instruction and data caches- FPU- Comparison of Pentium and Pentium pro architecture. Introduction to Pentium II, Pentium III and Pentium IV processors Introduction to Intel and AMD 64 bit architectures. RISC Architecture : Definition of RISC Properties of RISC Systems Practices in RISC Systems Register windowing Advantages and shortcomings Comparison with CISC architecture .

UNIT – IV

Intel 80x86 Programming: 80x86 Instruction set , Assembly level programming with DEBUG and MASM MS-DOS Functions and BIOS Calls - programming examples using 80x86.

UNIT – V

Introduction IBM PC Architecture , Peripherals & Interface Buses: Motherboard- Chip sets - graphic adapters and monitors-drive controllers - floppy and hard disk drives- IDE and SCSI - streamers and other drives -parallel interfaces and printers - serial interfaces 16550 UART CMOS RAM and real time clock- keyboard and mouse- the power supply (SMPS) - BIOS and Boot Process Bus Systems: PC/XT and AT Buses Microchannel and ISA Local Buses: VESA and PCI- I/O Buses: SCSI and USB

Text Books:

1. Barry B. Brey , The Intel Microprocessors 8086 to Pentum 4- Archetecture Programming and Interfaceing, 6/e Pearson Education ,2003.
2. James L. Antonacos , An Introduction to Intel Family of Microprocessors , 3/e Pearson Education, 2002.

Reference Books:

1. John Uffenbeck , The 80x86 Family Design Programming and Interfacing, 3/e Pearson Education, 2002
2. YU-Cheng Liu & Glenn A Gibson, Microprocessor System , Architecture Programming & Design, Pentice Hall of India.
3. Douglas V Hall, Microprocessors & Interfacing, Tata McGrahill, 1998
4. Intel Users manual for 8086, 80386 & 80486, Pentium processors
5. H. P. Messmer, The Indispensable PC Hardware Book, 3/e, Addison Wesley, 1997
6. S. J. Bigelow, Troubleshooting, Maintaining, and Repairing PCs, 2/e, Tata McGraw Hill, New Delhi, 1999
7. Ytha Yu and Charles Marut , Assembly Language Programming and Organisation of IBM PC, International Edition , McGrawhill Inc, 1992
8. K. Miller, An Assembly Language Introduction to Computer Architecture using the Intel Pentium, Oxford University Press, 1999.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. I Sem.** Branch: **Electronics & Telecom.**
Subject: **Digital Communication Techniques** Code: **555113 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02**

UNIT – I

Baseband and Bandpass Digital Transmission: Baseband modulation, Correlative coding, Detection of binary signals in Gaussian Noise, ISI, Eye pattern and equalization, Bandpass modulation techniques, coherent and noncoherent detection of signals in Gaussian noise, error performance for binary and M-ary signals.

UNIT – II

Source coding methods: Review of information theory, Huffman and L-Z encoding algorithm Rate distortion theory for optimum quantization, Scalar vector quantization.
Advanced transmission methods: The signal space concept, Gram-Schmitt procedure, signal space representation of modulated signals, nonlinear modulation method with memory, Error probability and optimum receiver for AWGN channel.

UNIT – III

Error Control Coding: Linear block codes, error detecting and correcting capability, cyclic codes, convolutional codes, properties of convolutional codes, Viterbi decoding algorithm, Turbo code concepts, Trellis codes.

UNIT – IV

Synchronization, Multiplexing and Multiple Access: Carrier and Symbol synchronization, Frequency Division Multiplexing/Multiple Access, Time Division Multiplexing/Multiple Access, performance comparison of FDMA & TDMA, Code Division Multiple Access, capacity of multiple access methods, Access algorithms: ALOHA, Slotted ALOHA, Reservation ALOHA, Carrier sense systems and protocols

UNIT – V

Spread Spectrum Techniques: Model of spread spectrum digital communication system, direct sequence spread spectrum system, frequency hopped spread spectrum system, generation of PN sequences, synchronization of spread spectrum systems.

Textbooks

J. G. Proakis, “Digital Communications”, Fourth Edition, McGraw Hill Inc.
Bernard Sklar, “Digital Communications: Fundamentals and Applications”, Second Edition, Pearson Education Asia (LPE)

Reference Books

Simon Haykin, “Digital Communications”, John Wiley and Sons
K Sam Shanmugam, “Digital Communications”, John Wiley and Sons
Modern communication systems (Principles and application), Leon W. Couch JI(PHI)
Digital communication: Simon Haykin (WEP)

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. I Sem.** Branch: **Electronics & Telecom.**
Subject: **VLSI Design** Code: **555114 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: 02

UNIT - I

MOS Transistor theory: n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter.

UNIT - II

CMOS Process Technology: Lambda Based Design rules, scaling factor, semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD. refractory gate, multilayer inter connect) , Circuit elements, resistor , capacitor, interconnects, sheet resistance & standard unit capacitance concepts delay unit time, inverter delays , driving capacitive loads, propagate delays, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, scaling of MOS circuits.

UNIT - III

Basics of Digital CMOS Design: Combinational MOS Logic circuits-Introduction, CMOS logic circuits with a MOS load, CMOS logic circuits, complex logic circuits, Transmission Gate. Sequential MOS logic Circuits - Introduction, Behavior of hi stable elements, SR latch Circuit, clocked latch and Flip Flop Circuits, CMOS D latch and triggered Flip Flop. Dynamic Logic Circuits - Introduction, principles of pass transistor circuits, Voltage boot strapping synchronous dynamic circuit techniques, Dynamic CMOS circuit techniques

UNIT - IV

CMOS Analog Design: Introduction, Single Amplifier. Differential Amplifier, Current mirrors, Band gap references, basis of cross-operational amplifier.

UNIT - V

Dynamic CMOS and clocking: Introduction, advantages of CMOS over NMOS, CMOS\SOS technology, CMOS\bulk technology, latch up in bulk CMOS., static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking- clock generation, clock distribution, clocked storage elements.

Text Books:

1. Neil Weste and K. Eshragian,"Principles of CMOS VLSI Design: A System Perspective," 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
2. Wayne, Wolf, "Modern VLSI design: System on Silicon" Pearson Education, Third Edition, 2005

Reference Books:

1. Douglas A Pucknell & Kamran Eshraghian, "Basic VLSI Design" PHI 3rd Edition (original Edition – 1994), 2005
2. Sung - Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", TMH, 2003 (Third Edition)
3. "Principles of CMOS VLSI Design " Neil Weste and Eshraghian (Second Edition) Pearson Education Asia (Addison – Wesley Publication Company
4. Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 2nd ed. New York : Oxford University Press, 2004.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. I Sem.** Branch: **Electronics & Telecom.**
Subject: **Fiber Optic Networks** Code: **555131 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: 02

UNIT - I
Introduction: Propagation of signals in optical fiber, different losses, nonlinear effects, solitons, optical sources, detectors.
Optical Components: Couplers, isolators, circulators, multiplexers, filters, gratings, interferometers, amplifiers.

UNIT - II
Modulation — Demodulation: Formats, ideal receivers, Practical detection receivers, Optical preamplifier, Noise considerations, Bit error rates, Coherent detection.
Transmission system engineering: system model, power penalty, Transmitter, Receiver, Different optical amplifiers, Dispersion.

UNIT - III
Optical networks: Client layers of optical layer, SONET/SDH, multiplexing, layers, frame structure, ATM functions, adaptation layers, Quality of service and flow control, ESCON, HIPPI.

UNIT - IV
WDM network elements: Optical line terminal optical line amplifiers, optical cross connectors, WDM network design, cost trade offs, LTD and RWA problems, Routing and wavelength assignment, wavelength conversion, statistical dimensioning model.

UNIT - V
Control and management: network management functions, management frame work, Information model, management protocols, layers within optical layer performance and fault management, impact of transparency, BER measurement, optical trace, Alarm management, configuration management.
Suitable number of Assignments / Tutorials can be given based on the syllabus

Text Books

1. John M. Senior, “Optical fiber Communications”, Pearson edition, 2000.
2. Rajiv Ramswami, N Sivaranjan, “Optical Networks”, M. Kauffman Publishers, 2000.

Reference Books:

1. Gerd Keiser, “Optical Fiber Communication”, MGH, 1 991.
2. G. P. Agarawal, “Fiber Optics Communication Systems”, John Wiley NewYork, 1997
3. P.E. Green, “Optical networks”, Prentice Hall, 1994.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. I Sem.** Branch: **Electronics & Telecom.**
Subject: **Reliability Engineering** Code: **555132 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: 02

UNIT-I
Basics of reliability: Mathematics of Reliability, Reliability function, Models of failure. Failure data Analysis, System reliability.

UNIT-II
Reliability models and systems: Basic Reliability Models, Covariate Models, Hazard Rate Functions including Exponential, Weibull, Normal and Lognormal, System Reliability including redundant, standby and load sharing systems,

UNIT-III
Reliability and failure: Failure mode, effect and criticality analysis, fault tree analysis, reliability and maintainability design methods based on availability and life cycle costs, Preventive maintenance

UNIT-IV
Failure preparedness: Spares Provisioning Models, Renewal and Minimal Repair Models, treatment of censored data, reliability growth testing, Probability Tests and curve fitting, Maintaining likelihood estimation and goodness of fitness tests, Series configuration. Parallel configuration r-out-of-n structure.

UNIT-V
Improvement and checks: Reliability improvement. Redundancy. Reliability allocation. Reliability testing.

Text Books:

1. An Introduction to Reliability and Maintainability Engineering - *Ebeling;* Tata McGraw Hill
2. Probabilistic Reliability - An Engineering Approach, *M.L. Shooman*, McGraw-Hill Publ

Reference Books:

1. Fault-Diagnosis Systems: An Introduction from Fault Detection to Fault Tolerance, *Rolf Isermann*
2. Engineering Design Reliability Handbook, *Boca Raton*; CRC Press

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. I Sem.** Branch: **Electronics & Telecom.**
Subject: **Parallel Processors** Code: **555133 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: 02

UNIT – I
Parallel Computer Models: The state of computing, multiprocessors and multicomputers, multivector and SIMD computers, architectural development tracks.

UNIT – II
Program and Network Properties: Conditions of parallelism, program partitioning and scheduling, program flow mechanisms. System Interconnect Architectures. Network properties and routing, static interconnection networks and dynamic interconnection networks, MPI and PVM architecture.

UNIT – III
Processors and Memory Hierarchy: Advanced processor technology- CISC, RISC, Superscalar, Vector, VLIW and symbolic processors, Memory hierarchy technology, Virtual memory technology (Virtual memory models, TLB, paging and segmentation)

UNIT – IV
Bus, Cache and Shared Memory: Cache memory organization, shared memory organization, sequential and weak consistency models.
Pipelining and Super scalar techniques: Linear Pipeline Processors, Nonlinear Pipeline processors, Instruction Pipeline Design, Arithmetic Pipeline Design

UNIT – V
Parallel and Scalable Architecture: Multiprocessors System Interconnects, Cache Coherence and Synchronization Mechanisms, Vector Processing Principles, Multivector Multiprocessors and Data Flow Architecture.

Text Books::

1. Computer Architecture and Parallel Processing*",* Kai Hwang, F. A. Briggs, McGraw Hill.

Reference Books:

1. Kai Hwang and Zu, “Scalable Parallel Computers Architecture”, McGraw Hill
2. M.Sasikumar, et.al., "Introduction to Parallel Processing", PHI, New Delhi, 2000
3. J .P.Hayes “Computer Architecture and Organization”, McGraw Hill.
4. Harvey G. Cragon, “Memory Systems and Pipelined Processors”, Narosa Publication.
5. V. Rajaranam & C.S.R. Murthy, “Parallel Computers”, PHI.
6. R. K. Ghose, Rajan Moona & Phalguni Gupta, “Foundation of Parallel Processing”, Narosa Publications.
7. Stalling W., “Computer Organization & Architecture”, PHI.
8. *M. J. Quinn, "Designing Efficient Algorithms for Parallel Computers", McGraw Hill International, 1994.*

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. I Sem.** Branch: **Electronics &Telecom.**
Subject: **Digital Instrumentation** Code: **555134 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02**

UNIT - I

Digital time measurement techniques : Vernier technique for small time interval measurement, Measurement of periodic time, Measurement of phase, capacitance, quality factor, time constant and decibel. **Digital frequency measurement techniques:** Measurement of ratio, product and difference between two frequencies, High frequency measurement, Peak frequency measurement, Fast low frequency measurement, Time reciprocating circuit.

UNIT – II

Automated Measurement Systems: Need and requirement of Automatic test equipment(ATE), Computer based & computer controlled ATE switches in ADTE, ATE for PCB, Component testing. IEEE –488 electronic instrument Bus standard, Field bus application.

UNIT-III

Computer control: Hierarchy of computer control for industry, Direct digital control, Distributed computer control: System architecture and implementation concepts, buses & communication networks of DCCS, SCADA system.

UNIT-IV

Intelligent controllers : Programmable logic controllers, PLC programming techniques, fuzzy logic controllers, Neural network controllers.

UNIT – V

Data Acquisition System: Microprocessor based data acquisition system; Signal conditioning, single channel data acquisition system, multi-channel data acquisition system, and data conversion using ADC and DAC in data acquisition system.

Text Books:

1. Applied Electronic Instrumentation and Measurement, 1992 by McLachlan & Buchla, Prentice Hall International
2. Digital Measurement Techniques, 1996 by T. S. Rathore, Narosa Publishers, New Delhi

Reference Books:

1. Electronic Instruments Handbook (3/e), 1997 by Clyde E. Coombs, McGraw Hill International
2. Sensors & Signal Conditioning, (2/e) 1994 by Pallas Areny and Webster, J.Wiley & sons
3. Digital Instrumentation, *Bouwnes*, Tata McGraw Hill Book Pub. Co.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. I Sem.** Branch: **Electronics &Telecom.**
Subject: **Advanced Digital Signal Processing Lab** Code: **555121(28)**
Total Practical Periods: **40**
Total Marks in end Semester Exam.: **75**

List of Experiments:

- To Generate the following waveforms
  - a: Unitstep Sequence
  - b. Ramp Sequence
  - c. Exponential Sequence
  - d. Sine Sequence
- Program for linear convolution
- Program of computing circular convolution.
- Program for computing cross correlation of the given sequence.
- Program for design of Butter worth LPF.
- Program for the design of FIR, LP, HP, BP and BS Filters using Rectangular Window.
- Program for estimating PSD of Two sinusoid Plus noise.
- Program for Drawn Sampling a Sinusoidal sequence by a faster M.
- Cancellation of echo produced on the telephone base band channel (Simulation).
- Program for the solution of normal equation using Levinson-Durbin Algorithms.
- Study of DSP Processor. (Texas Instrument)
- To Observe the effect of interpolation and decimation on the spectrum of a signal
- (DSP Works Software)
- To Generate and amplitude modulation Signal and observe the presence of sideband in its spectrum. (DSP works software)
- To Demonstrate Spectral Leakage.
- Program for partial fraction decomposition of a rational transfer function.

Recommended Books:

1. DSP – S Salivaliaran, A Vallavraj, TATA McGRAW HILL.
2. Digital Signal Processors - Architehure, Programming and Application- B Venkatramani, M Bhaskar, TATA MECGRAW HILL.
3. DSP – a Hands-on Approach – Charles schuler, Mahesh chugani, TATA McGRAW HILL

List of Equipments/Machines/Software etc.:

1. MATLAB Software with DSP Toolbox.
2. DSP_{works} Signal grneration and Analysis Software.
3. TMS 320C6** service starter Kits with Code composer Studio.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. I Sem.** Branch: **Electronics &Telecom.**
Subject: **Advanced Microprocessors & Interfaces Lab** Code: **555122 (28)**
Total Practical Periods: **40**
Total Marks in end Semester Exam.: **75**

List of Experiments:

- Study of 8086 microprocessor kit, its operation & commands.
- Write a well-documented program for copying 12 bytes from source to destination, on 8086 microprocessor kit.
- Write a program for 8086 for division of a defined double word (stored in a data segment) by another double word and verify.
- Write a well-documented program for finding the square root of a given number, on 8086, microprocessor kit.
- Write a program using 8086 for finding the square of a given number and verify.
- Write a program using 8086 and verify for:
    - Finding the largest number from an array.
    - Finding the smallest number from an array.
- Write a program using 8086 for arranging an array of numbers in descending order and verify.
- Write a program using 8086 for arranging an array of numbers in ascending order and verify.
- Write a program for 8086 for finding square of a number using look-up table and verify. .
- Write a program to interface a seven-segment LEDs.
- Write a program to control the operation of stepper motor using 8086 microprocessor.
- Write a program to simulate a traffic light control using microprocessor.
- Write an assembly language program using assembler to Edit an ASCII string.
- Write a program to interface a keyboard.
- Write a program to find the solution of a quadratic equation.

List of Equipments/Machines/Software etc.:
Microprocessor Kit, Microprocessor Simulator, Assembler, PCs, Interfacing Cards

Reference Book:
Douglas V Hall, Microprocessors & Interfacing, Tata McGrahill, 1998